REMARKS

Claims 1-48 have been canceled and claim 61 has been amended. Claims 49-69 are pending in the application. Reconsideration of the application is requested in view of the amendments and the remarks to follow.

The Examiner has required restriction between:

Group I: Claims 49-69; and

Group II: Claims 1-48.

Applicant elects the claims of Group I without traverse and cancels claims 1-48 without prejudice.

Claim 61 has been amended to address a minor informality noted during review, however, this amendment does not alter the scope of the claims. The amendments to the specification also address minor informalities noted during review. No new matter is added by the amendments to the specification or claims. The amendments to the specification and claims are supported at least by text appearing in paragraphs 18-38 of the application as originally filed.

Further, Applicant herewith submits a duplicate copy of the Information Disclosure Statement and Form PTO-1449 filed in this application on January 22, 2002. No initialed copy of the PTO-1449 has been received back from the Examiner. To the extent that the submitted references listed on the Form PTO-1449 have not already been considered, and the Form PTO-1449 has not been initialed with a copy being returned to Applicant, such examination

and initialing are requested at this time, as well as return of a copy of the initialed Form PTO-1449 to the undersigned.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

In view of the foregoing, allowance of claims 49-69 is requested. The Examiner is requested to phone the undersigned in the event that the next Office Action is one other than a Notice of Allowance. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: May 24, 2002 By: _____

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/056,179
Filing Date ..... January 22, 2002
Inventor ..... Weimin Li et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 2814
Examiner ..... Howard Weiss
Attorney's Docket No. MI22-1824
Title: Floating Gate Transistors and Methods of Forming Floating Gate Transistors

37 CFR § 1.121(b)(1)(iii) AND 37 CFR § 1.121(c)(1)(II) FILING REQUIREMENTS TO ACCOMPANY RESPONSE TO MAY 13, 2002 OFFICE ACTION

Deletions are bracketed, additions are underlined.

In the Specification

On page 6, paragraph 12 has been amended as shown below:

Fig. 7 is a cross-sectional representation of a portion of a semiconductor substrate of another exemplary embodiment of the present invention resulting from the substrate depicted in Fig. 5 and an alternate subsequent process stage.

On pages 8 and 9, paragraph 20 has been amended as shown below:

Fig. 1 is a cross-sectional representation of a portion of a semiconductor substrate 10 having patterned masking material portions 17 disposed over a semiconductive material 12. Material 12 includes an outermost surface 42. Patterned masking material portions 17 encompass masking portions 16 and can also include optional pad oxide portions 14. Masking portions 16 include outermost surface 40. By way of example, patterned masking material portions 17 can be formed by forming a masking material layer (not shown) over semiconductive material 12 and then employing a photo patterning and etch process to remove portions of such [first] masking material layer to define masking material portions 17. Where optional pad oxide portions 14 are desired, [such is] they are formed prior to the masking portions 16 and the resulting masking material portions 17 encompass both pad oxide portions 14 and masking portions 16. In some embodiments, a photoresist material employed in the photo-patterning and etch process is removed from over masking portions 16, in other embodiments, such photoresist material (not shown) is not removed. As shown, the photo patterning and etch process advantageously defines [an opening] openings 20 between [a pair] pairs of portions 17. Such provides but one example of forming [a first layer] the masking material 17 (here a composite of layers 14 and 16, with or without the photoresist material) [, and in the form of masking material,] over semiconductive material 12. [In another example of forming a first layer in the form of a masking material, a

photor sist material (not shown) utilized in the photo-patterning is not removed after the etching to form portions 17.]

On page 12, paragraph 26 has been amended as shown below:

In Fig. 5, a gate dielectric comprising a first dielectric layer 60 is shown formed over semiconductive material 12 and a conductive floating gate material layer 62 is shown formed over dielectric layer 60 and STI masses 24. In the exemplary embodiment of Fig. 5, conductive floating gate material layer 62 is formed with a thickness sufficient to completely fill recess 70.

On pages 16 and 17, paragraph 35 has been amended as shown below:

Fig. 11 is analogous to Fig. 5 where STI masses 24 of Fig. 5 are replaced with STI masses 24c as discussed above. Thus, first dielectric layer 60c is shown formed over semiconductive material 12 and conductive floating gate material layer 62c is shown formed over dielectric layer 60 and STI masses 24c. The exemplary embodiment of Fig. 11[,] depicts conductive floating gate material layer 62c formed with a thickness sufficient to completely fill recess 70c.

In th Claims

61. (Amended) A floating gate transistor structure, comprising:

a substrate comprising semiconductive material;

a pair of spaced shallow trench isolation (STI) masses having first portions received within the semiconductive material and second portions projecting outwardly from the semiconductive material, the first and second portions each having opposing sides, the opposing sides of the first portions defining an active area therebetween having a first cross-sectional dimension and the opposing sides of the second portions defining a region therebetween having a second cross-sectional dimension;

a first dielectric layer received within the region and overlying the active area;

a floating gate received within the region and overlying the [gate oxide] first dielectric layer;

a second dielectric layer overlying the floating gate; and

a control gate operatively overlying the second dielectric layer and operatively coupled to the floating gate.

Claims 1-48 have been canceled without prejudice.

END OF DOCUMENT